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TECHNICAL REPORT

Low cost FPGA based data acquisition system for a gamma imaging probe

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ABSTRACT: We present the development of a low cost field programmable gate arrays (FPGA) based data acquisition system for a gamma imaging probe proposed for sentinel lymph node (SLN) mapping. Radioguided surgery using a gamma probe is an established practice and has been widely introduced in SLN biopsies. For such applications, imaging systems require compact readout electronics and flexibility. Embedded systems implemented in the FPGA technology offer new possibilities in data acquisition for nuclear medicine imagers. FPGAs are inexpensive compared to application specific integrated circuits (ASICs), usually used for the readout electronics of dedicated gamma cameras and their size is rather small. In this study, cost effective analog to digital converters (ADCs) were used and signal processing algorithms were implemented in the FPGA to extract the energy and position information. The analog front-end electronics were carefully designed taking into account the low sampling rate of the ADCs. The reference gamma probe has a small field of view (2.5 cm $\times$ 2.5 cm) and is based on the R8900U-00-C12 position sensitive photomultiplier tube (PSPMT) coupled to a pixellated CsI(Na) scintillator with 1 mm $\times$ 1 mm $\times$ 5 mm crystal element size. Measurements were carried out using a general purpose collimator and ^{99m}Tc sources emitted at 140 keV. Performance parameters for the imaging gamma probe were compared with those obtained when data were acquired using the standard NIM (Nuclear Instrumentation Modules) electronics and found to be in very good agreement, which demonstrates the efficiency of the proposed implementation.

KEYWORDS: Digital signal processing (DSP); Front-end electronics for detector readout; Data acquisition concepts; Digital electronic circuits

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1 Introduction

Radioguided surgery is an innovative technique that provides surgeons with enhanced capabilities for accurate identification of structures of interest for excisional biopsy. The concept of this technique involves the use of a radiation detection system for the intraoperative detection of radionuclides. The use of gamma detection probe technology is a standard practice and has been widely introduced in sentinel lymph node (SLN) biopsies. SLN mapping can be useful in assessing the metastatic status of early-stage invasive breast cancer, and determining its prognosis and treatment options [1].

Several groups are developing dedicated cameras, suitable for SLN imaging [2]–[7]. The most important performance parameters of any given gamma detection probe system consist of:

- overall sensitivity (efficiency)
- spatial resolution
- energy resolution (spectral discrimination)

The combination of high sensitivity and high spatial resolution is the best solution for SLN mapping, but it possesses instrumentation challenges as those properties are competitive. In a previous work we have designed and optimized in terms of spatial resolution and sensitivity a gamma imaging probe for such an application [8]. Following its construction and performance evaluation, we studied the geometry of the optimal collimator-scintillator structure using Monte Carlo simulations. The system was modeled with the GATE toolkit and the simulation was validated by comparing GATE results with actual measurements. In this work, the data acquisition system (DAQ) used for the experiments was based on NIM (Nuclear Instrumentation Modules) electronics connected

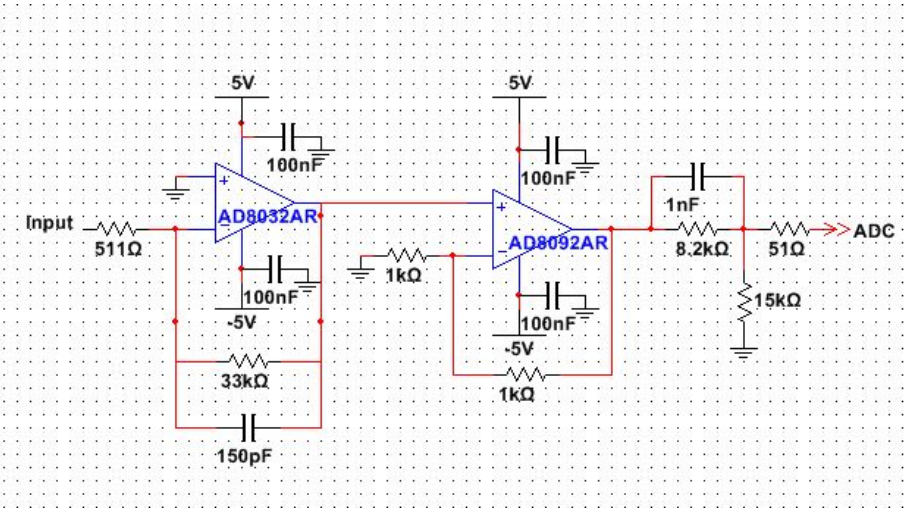

Figure 1. Preamplification circuit.

to a FAST multiparameter acquisition (MPA) system operating in the Windows 98 environment (MPA/WIN) [9]. Although this DAQ system was sufficient for validation, it is ineffective in terms of size and cost for the construction of a gamma detection probe. Apart from performance, the ergonomic design and overall cost of the imaging gamma probe are critical parameters for its clinical acceptance [10].

The aim of this work is the development of a compact, low cost and flexible data acquisition system for the imaging gamma probe described in [8]. Traditionally, custom made acquisition electronics, for such an application, are based on application specific integrated circuits (ASICs) [2–4]. However, we chose to implement the readout system in a simple and inexpensive FPGA evaluation board, while the digitization was performed using low cost free running ADCs. Compared to ASICs, the use of programmable technologies reduce the development time and risk while not significantly affecting the electronics size [11].

Performance parameters for the imaging gamma probe were measured using the proposed fully digital readout system and compared with those obtained when data were acquired using the NIM electronics. All measurements were performed using ^{99m}Tc sources. In this study the probe was coupled to a standard hexagonal collimator, while the pixellated scintillator was chosen to have 1 mm $\times$ 1 mm $\times$ 5 mm crystal element size, which is small enough, to test the performance of the readout system for small pixel identification.

2 Materials and methods

2.1 Scintillation detector

The imaging gamma probe is based on a Hamamatsu R8900U-00-C12 position sensitive photomultiplier tube (PSPMT) [12]. A CsI(Na) with 1 mm $\times$ 1 mm $\times$ 5 mm pixel size, 0.2 mm septa and 1 mm glass entrance window (Hilger, U.K.) is coupled to the PSPMT with optical grease (BC-630). The CsI(Na) array consists of 40 $\times$ 40 scintillator elements and its total size is 50 mm $\times$ 50 mm. The maximum emission wavelength of the CsI(Na) is at 420 nm [13]. A general purpose

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lead collimator with 1.5 mm hexagonal holes, 0.2 mm septa and 22 mm thickness was used in all experimental measurements. The optimal high voltage was found to be $= -980$ V for 140 keV excitation.

The R8900U-00-C12 has a square field of view (FOV) with external size 30 mm $\times$ 30 mm $\times$ 30 mm. The minimum effective area of the bialkali photocathode is 23.5 mm $\times$ 23.5 mm. The spectral sensitivity of the photocathode ranges from 300 nm to 650 nm with maximum absorption at 420 nm, which perfectly matches to the emission of CsI(Na) scintillator. Charge collection is carried out through an 11 metal channel dynode stage and a 6X+6Y cross plate anode.

2.2 Front-end electronics

The 6X+6Y anode signals are reduced to 2X+2Y (X_a, X_b, Y_c, Y_d) using a standard resistive chain [8]. Afterwards the four signals are fed to a custom preamplification circuit (figure 1) [14]. By using the anode division resistor chain the number of amplifiers and ADCs is significantly decreased, reducing system's cost and complexity, without loss in system's performance, as it has already been shown [8]. The flood image acquired with the NIM electronics show that even small crystals with less than the 1 mm $\times$ 1 mm cross-section can be resolved with the suggested readout scheme. In order to shape the analog signals, taking into account the ADC sampling rate, a high-pass filter has been added before the ADC, compared to the circuit presented in [8]. The pulse duration after the preamplification circuit was 12 usec and consists of 8 samples in its digitized form, for a sampling rate of 0.7 MHz (1.44 usec). A pole-zero cancelation adjustment was crucial for the proper baseline restoration. This filter was not necessary in the case of the NIM based data acquisition system used in [8], since a spectroscopy amplifier was used for the shaping of the analog inputs. For each scintillation event the four signals are summed, in order to obtain the entire energy information, while the position calculation is carried out by using the Anger logic:

$$x = \frac{X_a}{X_a + X_b}, \qquad y = \frac{Y_c}{Y_c + Y_d} \tag{2.1}$$

2.3 Digital readout electronics

2.3.1 Hardware description

In the current implementation the four position signals are continuously sampled using 12-bit, 0.7 MHz, free running ADCs from Digilent Inc [15] and read out by a XC3S500E Spartan 3E FPGA, provided in the Xilinx Starter Kit platform [16]. This board includes a 64 MByte DDR SDRAM external memory and a 10/100 Ethernet port, which are used for data storage and transmission.

The Xilinx embedded development kit (EDK, Xilinx Inc) was used for the design of the data acquisition system (figure 2). The overall architecture was developed, as an embedded system, using the Microblaze soft core processor. System's clock was 50 MHz. A custom core was written in VHDL (VHSIC Hardware Description Language) describing the digital processing of the acquired digitized data. Core's operation was verified using the ModelSim simulator (Mentor Graphics) and Chipscope Pro debugging tool (Xilinx Inc). All other interfaces are controlled via intellectual property (IP) cores provided by Xilinx. The custom core is connected to the external memory via a high speed port (Native Port Interface - NPI) provided in the Xilinx's memory controller (MPMC).

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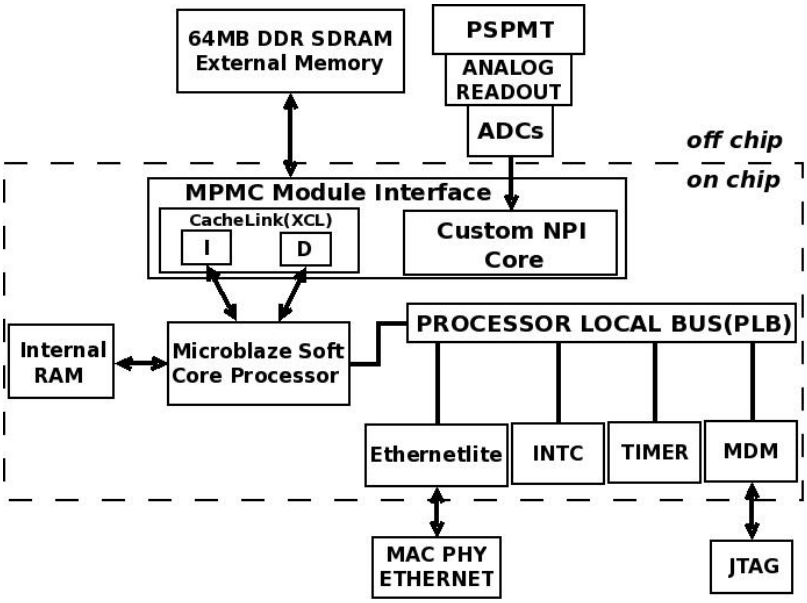

Figure 2. Block diagram of the embedded system.

In the current implementation, the MPMC is configured to have one more port. The Microblaze embedded processor uses the Xilinx CacheLink (XCL) port to access data and program stored in the DDR SDRAM memory. The embedded system contains also the following cores connected to the processor local bus (PLB):

- Ethernet controller (Ethernetlite)
- Interrupt controller (INTC)
- Timer
- Debug module for online debugging (MDM)

2.3.2 Acquisition method description

Analog signals are digitized using free running ADCs [17]. In free running sampling mode ADCs are clocked synchronously, while the analog signals are shaped taking into account the ADC sampling rate. The ADCs data are sent continuously to 4 shift registers, whose length depends on pulse width. For a sampling rate of 0.7 MHz (1.44 usec) and 12 usec pulse duration, 8×12 bits shift registers were implemented. A trigger signal is produced when the sum of the four ADCs samples exceeds a given digital threshold, implying the arrival of an event. The trigger is delayed by 6 ADC clock cycles to ensure that entire pulses are recorded. At that time, data are stored to a second set of registers while the first set is ready to accept the next event. An adder tree circuit was implemented, in order to calculate the integral of each pulse (X_a, X_b, Y_c, Y_d). A finite state machine was written in VHDL for the description of the NPI timing protocol [18], in order to write the four outputs to the external memory. The overall procedure, which is shown in figure 3, is quite simple and can be implemented in a FPGA with limited available resources.

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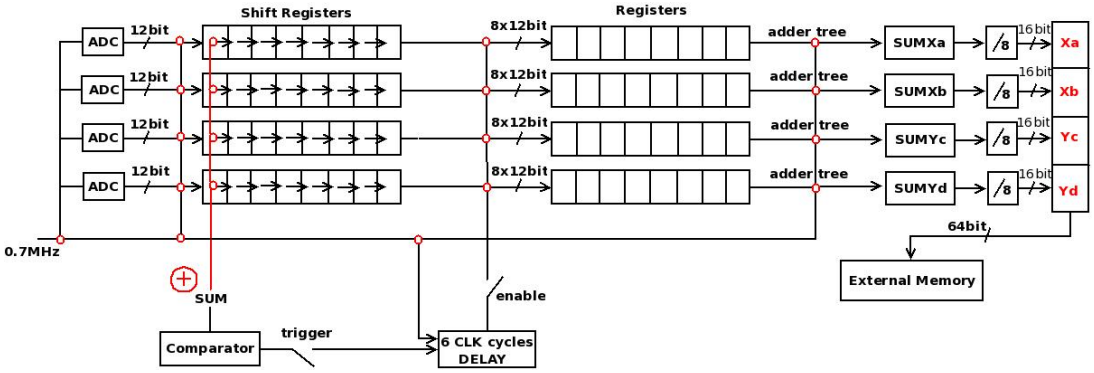

Figure 3. Block diagram of the custom core.

For every 1000 events stored in the memory, an interrupt signal occurs. Microblaze is programmed in C language to read data from memory at each interrupt and pass them to the lwIP networking stack [19], which is used for sending data to a server running on a linux machine, using the user datagram protocol (UDP). A timer is used to interrupt at a constant interval for sending the UDP datagrams. Custom software was developed to process and elaborate data for spectra analysis.

2.4 System performance

In order to evaluate the data acquisition architecture a set of experiments were carried out and the performance parameters were compared to those obtained with the NIM based data acquisition system [8].

Crystal mapping was achieved by placing a ^{99m}Tc point source, with 100uCi activity, at 300 mm above the scintillator without using a collimator. The average peak-to-valley ratio of a row profile in the flood image was calculated to assess the accuracy of crystal pixels mapping. The crystal look-up-table (LUT) was calculated to correct the intensity and energy non-uniformities of the raw images [20, 21].

The same setup was used to determine the intrinsic energy resolution. This value was calculated from the Gaussian fitting of the normalized energy spectrum, which is computed as follows: first, the LUT of each pixel position is extracted from the raw image and its energy spectrum is derived. Each spectrum is normalized to the same photopeak position (at ADC channel 50) by multiplying each value of the spectrum with the ratio of the normalized photopeak to the current photopeak. The normalized energy spectrum is then the sum of all individual spectra of the crystal elements.

The spatial resolution and sensitivity values were measured by linearly stepping a 20 mm long and 1 mm inner diameter, capillary source, filled with a 120uCi ^{99m}Tc solution, at different distances (0 to 50 mm) from the detector, above the collimator [22]. The full width at half maximum (FWHM) of the capillary tubes profiles were calculated using Gaussian fit. FWHM values (in mm) were extracted by multiplying the variance of the distribution σ with 2.35. All images were corrected using the LUT calibration files and an $\pm$10% energy window. Acquisition time, for spatial resolution and sensitivity measurements, was 300 sec.

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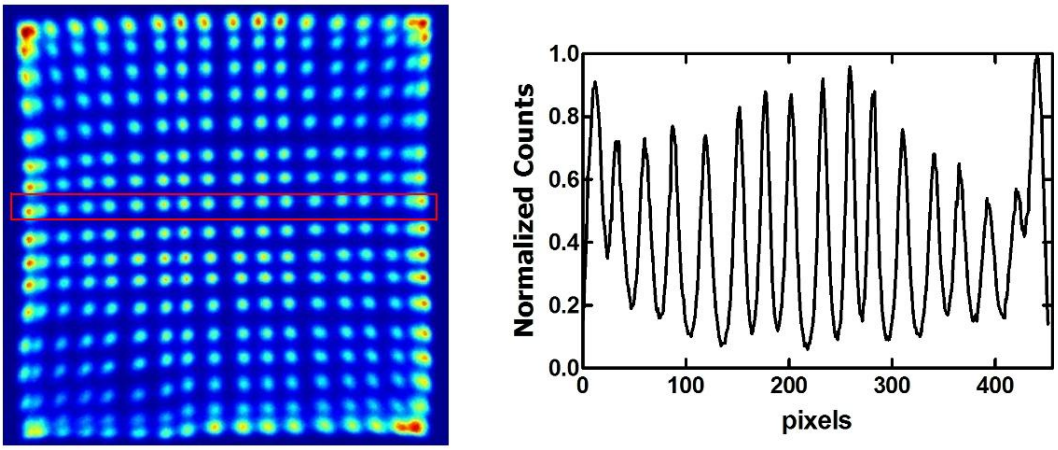

Figure 4. XC3S500E Spartan 3E readout: flood map (left), horizontal line profile (right).

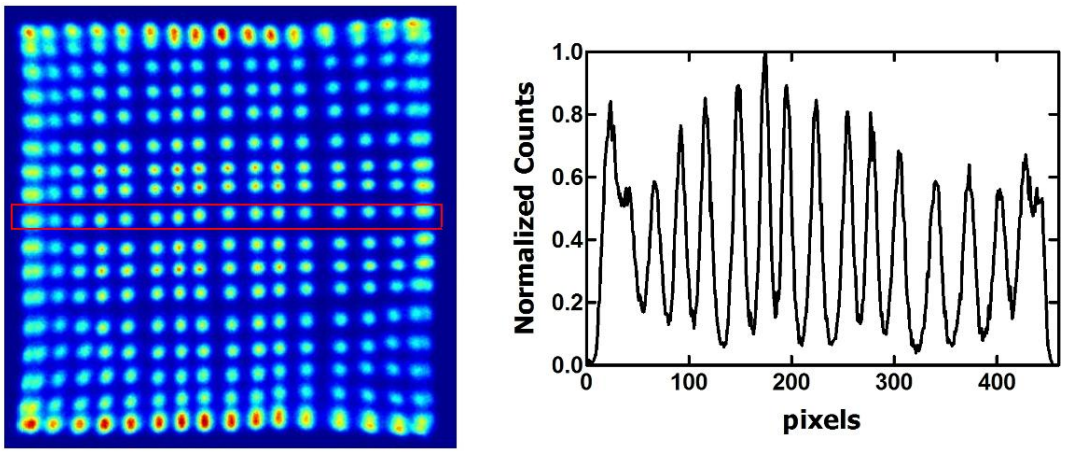

Figure 5. NIM electronics readout: flood map (left), horizontal line profile (right).

The data acquisition system is nonparalyzable [22]. The dead time of the system is 12 usec, which leads to a maximum count rate of 83333 cps, reasonable enough for SPECT applications. The achievable maximum data transfer rate with this architecture is 7.2 Mbps, fast enough as far as the maximum count rate of the system (1 event = 64 bits) is concerned.

3 Results and discussion

A raw flood ^{99m}Tc image and a horizontal row profile of the CsI(Na) 1 mm × 1 mm × 5 mm scintillator without collimator are illustrated in figure 4. The flood image shows a very good identification of crystal elements with 6:1 average peak-to-valley ratio. The expected number of pixels were identified, considering the effective area of the bialkali photocathode. The results are comparable with those illustrated in figure 5, which were presented previously in [8], using NIM electronics for the readout. The average peak-to-valley ratio in that case was 7:1.

Figure 6 shows the normalized energy spectra for the two readout systems. The mean energy resolution was measured equal to 28% for the FPGA based readout system, while the value

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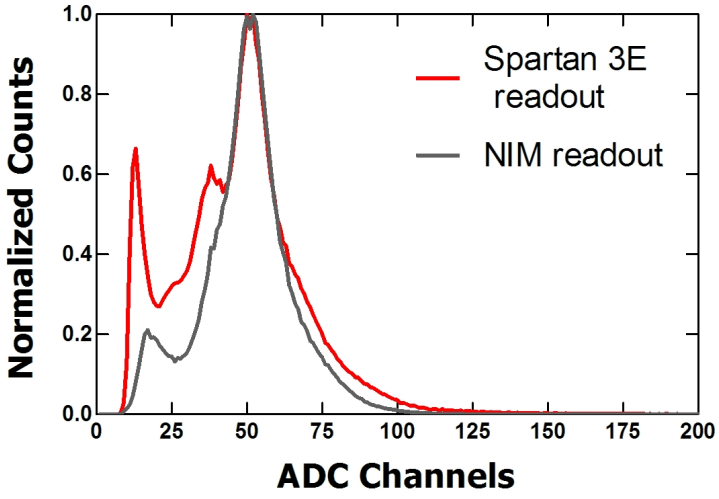

Figure 6. Normalized energy spectra for the two readout systems.

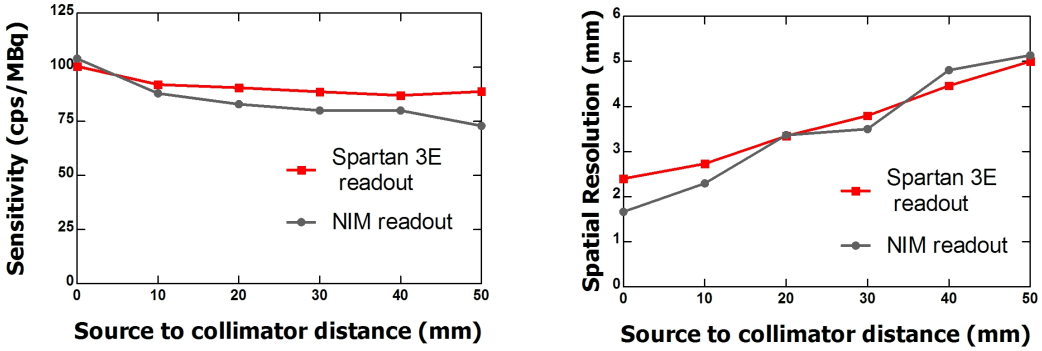

Figure 7. Sensitivity and spatial resolution, for the two readout systems, as a function of distance from the collimator.

achieved using the NIM electronics was 30% [8]. The spectra are quiet similar at the photopeak region, although the FPGA system includes more events at the lower channels, possibly due to the different lower energy threshold logic that we use.

Finally, figure 7 shows a comparison of the sensitivity and spatial resolution values measured for the two data acquisition systems, as a function of distance from the collimator. The sensitivity achieved was 90 cps/MBq, while the spatial resolution was found to be 2.3 mm at zero distance and ~ 5 mm at 5 cm from collimator respectively, for the proposed readout. In both cases there is good agreement between the FPGA and the NIM system presented in [8]. The agreement of the performance parameters between the XC3S500E Spartan 3E FPGA readout and the one using NIM electronics shows that the proposed system can be used for data acquisition in this probe.

The proposed architecture uses only a FPGA, four free-running ADCs, a DDR SDRAM memory, a physical ethernet port and a Universal Serial Bus (USB) port. All other board's peripherals

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are practically not used. In order to further reduce system's size, the proposed digital readout can be implemented in a custom board, which will contain only the necessary hardware. Our final goal is the construction of a miniaturized, low cost digital readout system, which will be connected to the optimized (in terms of crystal and collimator) probe and will be clinically evaluated.

4 Conclusions

A prototype of the digital readout electronics of an imaging gamma probe, for SLN mapping, has been designed and evaluated. The current implementation offers a compact, flexible and low cost solution for data acquisition of such imaging systems. We have chosen to implement the system in the simplest FPGA evaluation board of the market using low cost ADCs for the digitization. The ADC low sampling rate does not affect the overall performance of the system, as the measured parameters of interest are comparable with those obtained when data were acquired using NIM electronics. The analog front-end electronics were carefully designed, in order to acquire the whole PSPMT pulses despite the low sampling rate. The embedded system design is quite simple and can be implemented in a FPGA with limited available resources. The use of high speed ADCs along with a FPGA with more available resources may increase the performance of the system, however the goal of this study was to trade off between price and performance, keeping the first as low as possible.

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