

Dielectric characterization of macroporous thick silicon films in the frequency range 1 Hz–1 MHz

M. Theodoropoulou^{*, 1}, D. N. Pagonis¹, A. G. Nassiopoulou¹, C. A. Krontiras², and S. N. Georga²

¹ IMEL/NCSR Demokritos, Terma Patriarhou Grigoriou, Aghia Paraskevi, 15310 Athens, Greece

² Department of Physics, University of Patras, Patras 26504, Greece

Received 20 November 2007, revised 8 May 2008, accepted 13 May 2008 Published online 16 September 2008

PACS 73.40.Qv, 77.55.+f, 81.05.Rm, 85.30.De, 85.85.+j

* Corresponding author: e-mail mtheodo@imel.demokritos.gr, Phone: +00302106503137

Macroporous silicon was fabricated on selected areas on p⁺ silicon substrate by anodization in HF x Ethanol solution. Pore size was ~ 130 nm. By high temperature thermal oxidation, a thin SiO₂ layer was formed on pore walls. MOS capacitors with AI metallization were then fabricated and the samples were characterized by dielectric spectroscopy (DS) in the frequency range 1 Hz–1 MHz and in the temperature range 173–353 K. The results reveal that at low temperatures the dielectric constant ε' is independent of frequency ($t_{ox} = 20$ nm $\varepsilon' \sim 3.4$, $t_{ox} = 40$ nm $\varepsilon' \sim 2.8$, $t_{ox} = 72$ nm $\varepsilon' \sim 2.6$). A theoretical model, based on Vegard's law, which calculates the static dielectric constant of the samples, was used. The calculated theoretical values are in good agreement with the experimental results. Dielectric loss data show that the

oxidized samples exhibit values of $\tan \delta < 10^{-2}$ which are smaller than those of the non oxidized samples. The obtained dielectric characteristics enable oxidized macroporous silicon thick layers to be good candidates for use in RF isolation on a silicon substrate. Transient current measurements were also performed at room temperature for voltages from 1.0 to 20.0 V in the time interval 1-100s in accumulation. The analysis of the experimental data reveals that the conductivity is governed by two different conduction mechanisms. In the low applied voltage region the conduction is due to thermally excited electrons, hopping from one state to another. For higher voltages Fowler-Nordheim (F-N) tunnelling of electrons through the oxide prevails.

© 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

1 Introduction

Macroporous silicon (MacroPS) is an interesting material for applications in many different fields, including photonic crystals [1, 2], micro-array technology biochips [2], photovoltaic solar cells [3], capacitor technology [4], chemical sensors [5] etc. On-chip applications include both DC and RF isolation by silicon integrated porous silicon micro-plates. So far, for these last applications, mainly mesoporous silicon has been investigated [6-8]. The dielectric properties of both meso- and macroporous silicon depend strongly on the structural and morphological properties of the material. Surface oxidation has also a strong influence on these properties. Recently, there is a strong interest of using macroporous silicon in on-chip applications, since it exhibits very good mechanical properties and perfect stability with time. In this work, the dielectric proper-



ties of non-oxidized and oxidized macroporous silicon, fabricated on a highly doped p-type Si wafer and having pores with diameter ~ 130 nm, are investigated.

A powerful tool for the investigation of the electrical properties of materials is a combination of transient electrical conductivity and dielectric response measurements. Transient conductivity offers the ability to investigate the current versus applied voltage, through a device, as a function of time. Thus, the dc electrical behaviour of oxidized macroporous silicon can be investigated at each time instant after the application of the voltage. Dielectric response measurements allow the possibility of investigating bulk dielectric processes.

The dielectric properties of the samples of this work, were investigated over a wide range of frequencies (1 Hz– 1 MHz), temperature and oxidation conditions. The dielec-



tric properties of macroporous silicon, at frequencies higher than 1 MHz, were investigated elsewhere [9]. The determination of the conduction mechanisms at room temperature, responsible for the electrical properties of the oxidized macroporous silicon, is also reported.

2 Experimental

Macroporous silicon (MacroPS) composed of cylindrical macropores perpendicular to the surface was fabricated on selected areas on p+ silicon substrates (resistivity: 5mOhm.cm). An ohmic contact was formed on the backside of the wafers by boron ion implantation followed by evaporation of an Al layer. The anodization process was carried out in an HF:Ethanol solution (40%: 60% in volume) at a current density of 20 mA/cm². The anodization time was properly chosen so that the thickness of the porous silicon layers was 10 µm and the pore diameter ~130 nm. The end result was a porous silicon layer of porosity ~64%. The samples were oxidized at 900 $^{\circ}$ C in O₂ ambient for adequate times in order to form SiO₂ of 20, 40 and 72 nm on pore walls and sample surface. The oxidation time for obtaining the above SiO2 thicknesses was calibrated separately on a planar Si surface. A second Al layer was evaporated on the porous silicon layer and patterned in order to form a metal/porous silicon/p⁺-cSi capacitor. A schematic representation of the investigated samples is shown in Fig. 1. The dielectric properties of the PS structures were recorded using a high resolution dielectric analyzer (Alpha-N NOVOCONTROL) in the frequency range 1 Hz-1 MHz and in the temperature range 173-353 K automaticaly controlled by a QUATRO Cryosystem. Each sample was placed inside a sample cell in a parallel plate capacitor configuration. Measurements were recorded every 10 °C over the entire temperature range. The voltage oscillator level was kept constant at 0.1 V rms. The measurements of transient conductivity were performed at room temperature, from 1 to 100 s after the application of voltage in the voltage region from 1.0-20.0 V in accumulation (c-Si is connected to the positive output of the power supply). A detailed description of the experimental setup for the transient measurements can be found elsewhere [10].



Figure 1 Schematic representation of the oxidized porous silicon samples investigated.

3 Results and discussion

Figure 2 presents the dielectric constant ε' versus f at room temperature, for the samples with 20, 40 and 72 nm

thick oxide on a 10 µm thick MacroPS. It is obvious that the dielectric constant ε' has values of 3.4, 2.8 and 2.5 respectively and is independent of frequency in the frequency range from 1 kHz to 1 MHz. The inset shows the dependence on frequency of the non-oxidized MacroPS sample. In the low frequency region, an increase of ε' is observed, which is attributed to the contribution of space charge carriers to the total dielectric response [11]. The dependence of the dielectric constant ε' on frequency f as a function of temperature is shown in Fig. 3 for the sample with 72 nm oxide thickness on pore walls. At low temperatures (T < 303 K) ε' is independent of frequency in the whole frequency range investigated. Above a certain temperature and in the low frequency region ($<10^3$ Hz) the dielectric constant increases versus temperature. The same behavior is observed for all the samples investigated. This increase is attributed to space charge carriers, which results leakage currents, and the temperature at which ε' increases depends on the SiO₂ thickness (inset in Fig. 3).



Figure 2 ε' vs. *f* at *T* = 303 K for the samples 20, 40 and 72 nm oxide thickness on pore walls and in the frequency range 1 kHz–1 MHz.



Figure 3 ε' vs. *f* as a function of temperature for the sample of 72 nm oxide thickness on pore walls. The inset shows ε' vs *f* at T = 303 K for samples with 40 and 72 nm oxide thickness.

Figure 4 presents $\tan \delta$ versus *f* at room temperature, for the samples with 20, 40 and 72 nm thick oxide on a 10 μ m

thick MacroPS. It is obvious that all oxidized samples exhibit values of $tan\delta$ from $10^{-1}-10^{-3}$ in the frequency range used. The inset shows the dependence on frequency of the non-oxidized MacroPS. The values of $tan\delta$ for all the oxidized samples are smaller than those of the non-oxidized ones, which makes the oxidized samples more appropriate for use as low-loss isolation micro-plates.



Figure 4 tan δ vs. *f* at *T* = 303 K for the samples 20, 40 and 72 nm oxide thickness on pore walls and in the frequency range 100 Hz–1 MHz.

For the analysis of the experimental data of the dielectric response, a theoretical model is proposed, which calculates the static dielectric constant. The dielectric constant of the oxidized MacroPS ε_{MPS} can be calculated using Vegard's law. In this model, two capacitors are connected in parallel. One is composed of "air" and the other is composed of a combination of Si and SiO₂. This Si/SiO₂ combination is called "solid phase" (Fig. 5a):

$$\varepsilon_{MPS} = \varepsilon_{air} P + \varepsilon_{SP} (1 - P) \tag{1}$$

where, *P* is the porosity of the non oxidized MacroPS. The dielectric constant of the "solid phase", ε_{SP} , can be calculated by considering two parallel capacitors with dielectrics Si and SiO₂, connected in series with a capacitor composed of SiO₂. This capacitance is negligible, due to the fact that it is very large and it is connected in series to the circuit (Fig. 5b):

$$\varepsilon_{sp} = \varepsilon_{Si} - \left(\frac{2t_{ox}}{t_{Si} + 1.1t_{ox}}\right) (\varepsilon_{Si} - \varepsilon_{ox})$$
For $t_{ox} = 0 \rightarrow \varepsilon_{sp} = \varepsilon_{Si}$,
For $t_{sp} = 2t_{ox} \rightarrow \varepsilon_{sp} = \varepsilon_{ox}$.
$$(2)$$

where, t_{Si} is the silicon thickness measured by SEM and t_{ox} is the oxide thickness (Fig. 6). From Eqs. (1) and (2), the static dielectric constant of the oxidized MacroPS can be calculated. Table 1 presents the experimental and the calculated values of dielectric constant of all the samples in-

vestigated. A good agreement between experimental and calculated values is observed.



Figure 5 Equivalent circuits for the theoretical calculation of the dielectric constant of oxidized macroporous silicon.



Figure 6 Cross section representation of the interior of a pore.

Table 1 Experimental and calculated values of the static dielectric constant of all the samples investigated.

$t_{ox}(nm)$	\mathcal{E}_{sp}	ε_{MPS} (theor.)	$\varepsilon_{MPS}(exp.)$
0	11.7	5.0	5.36
20	8.4	3.7	3.4
40	6.4	2.9	2.8
72	4.3	2.2	2.5

The time dependence of the transient current in a $\log I$ vs $\log t$ presentation in accumulation for different applied voltages and for the sample with 72 nm thick oxide, is presented in Fig. 7. The power law of dielectric universal response [11, 12], expressed through the relation

$$I = \alpha t^{-m} \tag{3}$$

where α and *m* are constants, is followed for all the samples. In order to investigate the electrical conduction mechanisms, the transient current I_{tr} versus the applied voltage *V* is shown in Fig. 8 at the time instant 100 s after the application of the voltage, in accumulation and at room temperature. For the sample with 72 nm thick oxide, the slope in a log-log plot is calculated to be ~1.0 in the whole voltage range used. This leads to the conclusion that the conductivity is ohmic [13–15]. As the thickness of the oxide layer decreases, another conduction mechanism prevails. In particular, for the sample with 40 nm thick oxide, the ohmic conduction mechanism prevails in the voltage range from 1.0–12.0 V (straight line in Fig. 8), while for



higher voltages an increased current is observed through the oxide due to the onset of F-N tunnelling of electrons [16]. For the sample with 20 nm thick oxide the ohmic conduction mechanism prevails in the voltage range from 1.0-6.0 V (straight line in Fig. 8) and the F-N tunnelling begins to prevail above 6.0 V. For clarity reasons, the inset shows the F-N plot for the sample with 20nm thick oxide in the voltage region from 6.0-12.0 V.



Figure 7 Time dependence of the transient current I_{tr} as a function of the applied voltage in accumulation for 72 nm oxide thickness on pore walls.



Figure 8 Voltage dependence of the transient current at the time instant t = 100 s in accumulation. The inset shows the F-N plot for the sample with 20 nm oxide thickness on pore walls in the voltage region from 6.0-12.0 V at room temperature.

4 Conclusions

Macroporous silicon was fabricated on selected areas on p^+ silicon substrate by anodization. A thin SiO₂ layer was then formed on pore walls by high temperature oxidakHz to 1 MHz and it has values of 2.5, 2.8 and 3.4 for the samples with respectively 72, 40 and 20 nm thick SiO₂ layer on pore walls. The static dielectric constant of the samples was calculated. The calculated theoretical values are in good agreement with the experimental ones. All oxidized samples exhibit values of tan δ from 10^{-1} to 10^{-3} in the frequency range used. The obtained dielectric characteristics of the samples showed that oxidized macroporous silicon thick layers are good candidates for use in low-loss isolation applications intergrated on Si. The voltage dependence of the current shows two conduction mechanisms depending on the oxide thickness. For low voltages the conduction mechanism is ohmic and can be attributed to electrons hopping from one state to the other. In the high voltage region the prevailing conduction mechanism is F-N tunneling of electrons through the oxide. F-N conduction mechanism begins to prevail at smaller applied voltages as the thickness of the SiO₂ decreases.

tion. The dielectric constant of oxidized MacroPS samples

is frequency independent in the frequency region from 1

References

- A. Birner, R. B. Wehrspohn, U. M. Gosele, and K. Busch, Adv. Mater. 13(6), 277 (2001).
- [2] V. Lehmann, phys. stat. sol. (a) 197(1), 13 (2003).
- [3] C. Levy-Clement, S. Lust, S. Bastide, Q. N. Le, and D. Sarti, phys. stat. sol. (a) **197**(1), 27 (2003).
- [4] V. Lehmann, in: Properties of Porous Silicon, edited by L. Cahnam, EMIS Datarev. Ser. No. 18, 390 (1997).
- [5] R. Angelluci, A. Poggi, L. Dovi, G. C. Cardinali, A. Parisini, A. Tagliani, M. Mariasaldi, and F. Cavani, Sens. Actuators A 74, 95 (1999).
- [6] H. S. Kim, K. Chang, and Y. H. Xie, phys. stat. sol. (a) 197(1), 269 (2003).
- [7] H. Contopanagos and A. G. Nassiopoulou, Solid State Electron. 50, 1283 (2006).
- [8] D. N. Pagonis, G. Kaltas, and A. G. Nassiopoulou, J. Micromech-Microeng. 14(1-5), 793 (2004).
- [9] H. Contopanagos, D. N. Pagonis, and A. G. Nassiopoulou, phys. stat. sol. (c), submitted.
- [10] S. N. Georga and M. N. Pizanias, J. Phys. D 16, 1521 (1983).
- [11] A. K. Jonscher, Dielectric Relaxations in Solids (Chelsea Dielectrics Press, London, 1983).
- [12] P. K. Karahaliou, M. Theodoropoulou, C. A. Krontiras, S. N. Georga, N. Xanthopoulos, M. N.Pizanias, M. Kokonou, A. G. Nassiopoulou, and A. Travlos, J. Appl. Phys. 95(5), 2776 (2004).
- [13] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1981).
- [14] M. Theodoropoulou, P. K. Karahaliou, C. A. Krontiras, S. N. Georga, N. Xanthopoulos, M. N. Pizanias, C. Tsamis, and A. G. Nassiopoulou, J. Appl. Phys. 96(12), 7637 (2004).
- [15] M. Theodoropoulou, C. A. Krontiras, S. N. Georga, N. Xanthopoulos, M. N. Pizanias, C. Tsamis, and A. G. Nassiopoulou, Mater. Sci. Eng. B 101, 334 (2003).
- [16] D. K. Schroder, Semiconductor Material and Device and Characterization, 2nd ed. (Wiley, New York, 1998).