

Probing the Electrical Properties of the Si Nitride/Si Interface

C. Tsonos, A. Kanapitsas, A. Karagounis, I. Stavarakas, D. Triantis, C. Anastasiadis, P. Photopoulos, V. Em. Vamvakas and P. Pissis

Abstract - The present publication employs Dielectric Relaxation Spectroscopy for the examination of the relaxation mechanisms in silicon nitride MIS structures. These results are combined with capacitance and conductance measurements in order to give a more complete picture of the dielectric behaviour of silicon nitride. The analysis concludes with a method based on Dielectric Relaxation Spectroscopy for the calculation of the depletion layer width.

I INTRODUCTION

Silicon nitride is material widely used in microelectronics. Some of its applications include Si_3N_4 films as gate dielectrics in MOS transistors [1] or in MOS ICs in the form of thin nitride-oxide layers [2] for memory applications. Because of these and other applications the dielectric properties of Si_3N_4 have been extensively studied [3,4].

The calculation of the depletion width for an MIS structure, a p-n or a Schottky diode, is based on the solution of the Poisson equation by making some approximations based on the relative magnitudes of the carrier concentrations and the impurity concentrations in the depletion region. In all these cases the depletion width w of the induced space charge depletion region, is proportional to $V^{1/2}$, where V is the built in voltage V_{bi} for the case of p-n diodes or the potential drop across the semiconductor, usually denoted by Ψ_s , for the case of a MIS structure [5]. The above dependence assumes a crystalline and uniformly doped semiconductor, and finds that in the full depletion approximation the magnitude of the net charge density in the depletion region is equal to the product of the unit charge and the dopant density. Nonetheless determining the width of the depletion region is not always straight forward especially for some novel structures and devices. One example is organic semiconductor structures. This is because of the fact that density of the trapped charges in such structures is not

constant within the depletion region and changes with the bias voltage; consequently Poisson's equation has to be solved numerically to obtain the depletion width [6]. To do so, the density of states in the organic is required, which is strongly dependent on the molecular order in the semiconductor. An experimental method has been recently proposed by Takshi et. al. [7] where it was found that the depletion width does not follow the square root law dependence on applied voltage.

In a different type of application, the width of the depletion region affects the efficiency of solar cells. In a recent publication Eun-Chel Cho et. al. [8] reported the fabrication of silicon quantum dot/crystalline silicon solar cells. In such devices the calculation of the depletion width is not a straightforward issue but it does play a critical role in the efficiency of the solar cells. Finally, accurate knowledge of the depletion layer width is also necessary in the case of reliability tests in MOSFET devices.

II DEVICE LAYOUT AND EXPERIMENTAL TECHNIQUES

MIS devices were fabricated by Al deposition (11 mm in diameter), over a 99 nm thick Si_3N_4 layer grown on a 380 μm thick n-type Si substrate. Ohmic contacts were formed on the Si-substrate by aluminum alloying. Detailed description of the growth of the Si_3N_4 film has been reported in previous work [10]. A Novocontrol Alpha Analyser in combination with the Novocontrol Quatro Cryosystem was used for the Capacitance – Voltage (C-V), Conductance – Voltage (G-V) and Dielectric Relaxation Spectroscopy (DRS) measurements. For the C-V and G-V measurements the applied voltage ranged from -15 V to +15 V with steps of 0.5 V (and 0.1 V in depletion region) in the frequency range 1 kHz – 100 kHz, while the DRS measurements were carried out in the frequency range 10 Hz – 1MHz. All measurements have been carried out at room temperature, 300 K.

III RESULTS AND DISCUSSION

In order to identify the accumulation-depletion-inversion regions of the device, the capacitance-voltage and conductance-voltage characteristics for various frequencies were determined simultaneously. Fig. 1 depicts the C-V curves for the silicon nitride MIS structure with

C. Tsonos, A. Kanapitsas, and A. Karagounis are with the Electronics Department, Technological Educational Institute of Lamia, 35100 Lamia, Greece, E-mail: tsonos@teilam.gr,

I. Stavarakas, D. Triantis, C. Anastasiadis, P. Photopoulos are with the Electronics Department, Technological Educational Institute of Athens, 12210 Athens, Greece,

V. Em. Vamvakas is with the HelioSphera S.A. Building Block 8, Street 5, Industrial Area of Tripolis, 22100, Tripolis, Greece, and

P. Pissis is with the Physics Department, National Technical University of Athens, 15780 Zografou, Athens, Greece.

frequency as a parameter. The data were first corrected for series resistance [11]. The three regimes of accumulation, depletion and inversion appear.

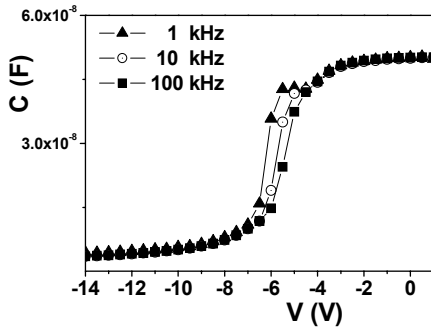


Fig. 1 C –V measurements at different frequencies.

A number of different methods have been used to measure D_{it} from the capacitive and conductive response of the interface states to a small ac signal [5].

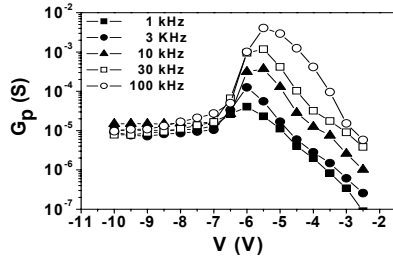


Fig. 2 G –V measurements at different frequencies.

Fig. 2 shows the conductance –voltage curve at different frequencies. The values were corrected for dc leakage. The peak corresponds to the depletion area of the device and its existence verifies the presence of interface traps. The curves verifying the MOS behaviour with interface states present [12]. A fast and reliable way to determine the density of the interface states (D_{it}) is the Hill-Coleman method [13]. According to this method, D_{it} can be calculated using the following relation

$$D_{it} = \frac{2}{qA} \frac{G_{m \max} / \omega}{[(G_{m \max} / \omega C_{ox})^2 + (1 - C_m / C_{ox})^2]} \quad (1)$$

where, A is the area of the device, ω is the angular frequency, $G_{m \max}$ is the maximum measured conductance value, C_{ox} is the capacitance in accumulation area and C_m is the capacitance value, which corresponds to the $G_{m \max}$ value. This method is very useful in understanding the electrical quality of the interface and the obtained values of the interface states for different frequencies are shown in Table I. The values of D_{it} depicted in Table I are not high, thus the interface defects cannot prevent the construction of an MIS device [14].

TABLE I. D_{it} AT DIFFERENT FREQUENCIES

Frequency (kHz)	3	10	30	100
D_{it} ($\times 10^{11}$ eV ⁻¹ cm ⁻²)	5.83	3.17	3.46	5.34

Admittance spectroscopy can identify both bulk and interface defects when used in MIS devices and in particular when the diodes are biased in depletion and a superimposed ac signal is applied across the diode terminals [12]. There are various models, which connect the measured G_p/ω versus frequency curves, with the density of interface states such as the discrete, the continuum and the statistical model [12]. One other model, the so called ‘extended tunneling’, is a combination of the continuum and the tunneling model and it has been applied in the past to fit successfully obtained data for various MIS structures [15-17]. The total parallel conductance, according to the ‘extended tunneling’ is given by the following relation

$$\frac{G_p}{\omega} = \frac{qD_{TS}}{2\omega\tau_{TS}} \ln[1 + (\omega\tau_{TS})^2] + qD_{TI} \int_0^d \frac{\ln[1 + (\omega\tau_0 e^{2K_1 x})^2]}{2\omega\tau_0 e^{2K_1 x}} dx \quad (2)$$

The subscripts TS and TI distinguish between interface traps in the semiconductor (in cm⁻².eV⁻¹) and traps in the insulator (in cm⁻³.eV⁻¹) respectively. The first term in the above sum corresponds to the capture and emission of electrons or holes described by the Shockley – Read-Hall (SHR) process, while the second expresses the tunneling of carriers from the interface states to the bulk of the insulator. The parameter d describes the effective tunneling distance of the electrons in the insulator x is the distance inside the insulator measured from the Si/nitride interface, τ_0 describes the time constant of the states at the interface while K_1 is the wave – vector of the electrons inside the insulator. It must be noted only the Eq. 2 can fit better our G_p/ω versus frequency curves, especially for the lower frequency data. Figure 3 shows the best fitting of Eq. 2 to the G_p/ω versus frequency curve with bias voltage –6 V. In the same plot of Figure 3 the contributions of each term of Eq. 2 are also presented. Representative results obtained from the best fitting of Eq. 2, in depletion region, are summarized in Table II.

TABLE II. FITTING PARAMETERS ACCORDING TO EQUATION 2

V_{bias} (V)	τ_{TS} (μ s)	$D_{TS} \times 10^{10}$ (cm ⁻² .eV ⁻¹)	d (nm)	τ_0 (μ s)	$D_{TI} \times 10^{12}$ (cm ⁻³ .eV ⁻¹)
-6	51	6.02	2.1	290	2.40
-5.7	17	8.75	1.9	23	2.37
-5.4	5	11.0	1.9	8.8	1.80

The comparison of the D_{TS} values presented in Table II, and these from Table I which based to the Hill-Coleman method, shows that the values of D_{TS} based to the ‘extended tunneling’ were found 3-9 times lower than the others. It is important also to mention here that, according to Table II, τ_0 is slightly larger than the τ_{TS} which means the SHR process occur slightly faster than the tunneling process. The previous behaviour was found in different MIS structures and is consequence of the connection between the measured conductance and the quantum phenomena occurring [17].

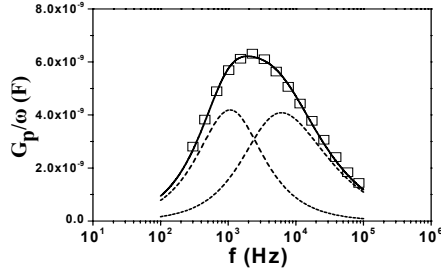


Fig. 3 G_p/ω vs. f for bias voltage -6 V and the best fitting curves.

The results of Dielectric Relaxation Spectroscopy (DRS) measurements can be described as functions of frequency via various formalisms. When conductivity relaxation mechanisms are studied by DRS and our interesting is focused to their capacitance, then the complex electric modulus M^* is the proper formalism to extract useful information [9]. In the case of a relaxation mechanism with a single relaxation time τ , the contribution to the real part of M^* is $\Delta M' = C_o/C$, where C is the capacitance associated with the regions where relaxation takes place, C_o is the geometrical capacitance and M''_{max} the maximum peak value of the imaginary part of M^* .

The dependence of the imaginary part of the electric modulus, M'' , on frequency is shown in Figure 4 at several bias voltage, 0 V corresponds to the accumulation region and -5.7 V, -6.0 V corresponds to the depletion region. For bias voltage 0 V only one peak appears in the frequency spectrum which present maximum at frequency around 50 Hz. From the peak maximum value, M''_{max} , and the geometrical characteristic of the nitride, a value of dielectric constant $\epsilon=6$ is extracted via the relation $C = \epsilon\epsilon_o A/t$, where A is the surface area and t is the thickness of the nitride. This value of dielectric constant is in full agreement with the corresponding measuring value from DRS, ~ 6 (see Figure 6). This means that the low frequency peak (Fig. 4) is related to the conductivity relaxation mechanisms which take place in the nitride. Impedance measurements support this finding. As it is seen in $M'' = M''(f)$ plots of Fig. 4, another relaxation mechanism appears at higher frequencies. The higher frequency relaxation should be related to the depletion region. This peak shifts gradually to lower frequencies as the bias voltage decreases. Also, (Fig. 4) the amplitude of the low frequency peak increases gradually which indicates a decreases of the total capacitance of MIS structure for bias voltage corresponding to the depletion region.

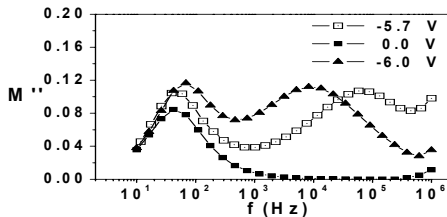


Fig. 4 M'' vs. f for different bias voltage.

To the $M'' = M''(f)$ plots, a sum of two empirical Havriliak – Negami (H-N) model equations were fitted [9]

$$M'' = \sum_{i=1}^2 \text{Im} \left[\frac{\Delta M'_i}{(1 + (i\omega\tau_{oi})^{1-\alpha_i})^{\beta_i}} \right] \quad (3)$$

where $\Delta M' = M'_{\infty} - M'_s$, $M'_{\infty} = 1/\epsilon'_{\infty}$, $M'_s = 1/\epsilon'_s$, $\tau_o = 1/2\pi f_o$ where f_o is a characteristic frequency that is closely related to the frequency where M'' attains a maximum at f_{max} . In the case of Debye or Cole – Cole shape $f_o = f_{max}$. Figure 5 shows a representative best fit of Eq. (3) to the experimental data of -5.7 V bias voltage. The plot shows not only the total fitting according to Eq. (3) but also the contribution of each relaxation. The fitting parameters for the lower frequency peak (nitride) are: $\alpha=0$, $\beta=0.96$, $f_o=46$ Hz and $\Delta M'=0.203$ while for the higher frequency peak (depletion region) they are: $\alpha=0.42$, $\beta=1$, $f_o=69.43$ kHz and $\Delta M'=0.433$. The lower frequency peak exhibit nearly Debye behaviour ($\alpha=0$ and $\beta \approx 1$), its f_{max} remain around 50 Hz while $\Delta M'$ values are in the range 0.194 – 0.203. The higher frequency relaxation presents Cole – Cole behaviour ($\beta=1$) with the values of parameter α in the range 0.39 – 0.44 and its $\Delta M'$ values in the range 0.426 – 0.465.

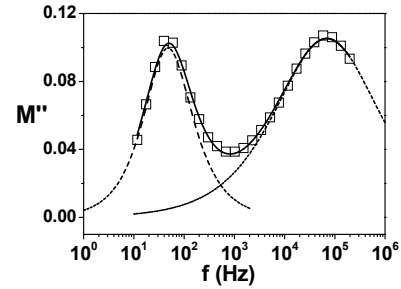


Fig. 5 M'' vs. f for -5.7 V bias voltage and the fitting curves.

As already has been mentioned earlier, the mechanism without polarization voltage (Fig. 4), corresponds to the conductivity relaxation mechanism of the nitride and it has $\Delta M'=0.17$. In the depletion region one can observe a rise of $\Delta M'$ due to the fact that the capacitance of this region is in a series connection with the capacitance of the nitride. The low frequency mechanism, in the depletion region bias voltage (Fig. 4), is the conductivity relaxation mechanism of the nitride relevant to the whole MIS structure (depletion region capacitance + nitride capacitance). The total capacitance C_l of the low frequency mechanism is

$$\frac{1}{C_l} = \frac{1}{C_i} + \frac{1}{C_d} \Rightarrow C_l = \frac{C_i C_d}{C_i + C_d} \quad (4)$$

where C_i and C_d are the capacitances of the nitride and the capacitance of the depletion region respectively. The value of C_i is equal to $6 \cdot C_o = 50.9$ nF.

The low frequency relaxation mechanism, present nearly Debye behaviour, which means that it is characterized from a single relaxation time, $\tau = 1/2\pi f_{max}$. For the low frequency relaxation at 0 V bias voltage it is $\Delta M'_i = C_o/C_i$ (C_o is the geometrical capacitance with $t=99$ nm), while for the same mechanism with bias voltage corresponding to the depletion region is $\Delta M'_i = C'_o/C_i$ (C'_o

here is the geometrical capacitance with $t=(99+w)$ nm, where w is the width of the depletion region). Dividing the two previous relations and taking into account the known values of $\Delta M_1'$, $\Delta M_h'$ and C_i , the thickness of the depletion layer width was found to be in the range of 15 nm – 18 nm. For this calculation, a value of dielectric constant of the higher frequency relaxation of $\epsilon_r=2.8$ was used. This value corresponds to the contribution to the real part of the complex dielectric constant ϵ^* of the higher frequency mechanism (Figure 6). In what follows, because the values of the depletion width w are already known, the values of C_l can be calculated easily by using Eq. (4). C_l varies from 36.4-38.2 nF for bias voltage varying from -5.5 V up to -6.0 V.

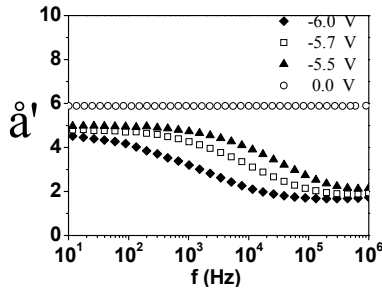


Fig 6. ϵ' vs. f for different bias voltage.

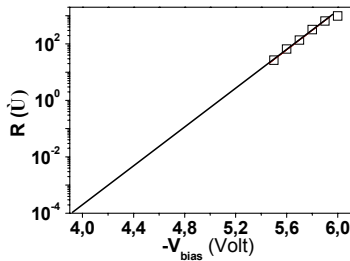


Fig 7. The resistance of the depletion region as a function of bias voltage.

Lets study now the high frequency mechanism. In a similar way as it has been presented earlier, by dividing the relations $\Delta M_1' = C_o' / C_l$, $\Delta M_h' = C_o' / C_h$ and taking into account the known values of $\Delta M_1'$ and $\Delta M_h'$ the capacitances C_h appear to have values in the region 16.0 - 17.3 nF. If R is the resistance of the higher frequency relaxation, then $\omega_{max} \cdot \tau = 1$, where $\omega_{max} = 2\pi f_{max}$ and τ is the characteristic relaxation time (mean relaxation time), $\tau = RC$. From the previous relation, the resistance R is calculated as a function of V_{bias} (Fig. 7). The gradual increase of R is observed as $-V_{bias}$ increases. Also, a tendency for saturation is observed when the silicon surface is depleted or weakly inverted, at -6 V.

Supposing that the linear behavior observed in Fig. 7 is also valid for values of the voltage higher than -5.5 V, then the extrapolation of the linear approximation $\log R = -16.35 + 3.25 \cdot (-V_{bias})$ for $R = 10^{-4} \Omega$ corresponds to a value of the bias voltage very close to -4 V. The value $R = 10^{-4} \Omega$ corresponds to the resistance, if the depletion layer behaves like the Si wafer with resistivity value 50 $\Omega \cdot \text{cm}$. So, the Si region which corresponds to the high frequency mechanism

starts to show a different electrical behavior at a bias voltage value of about -4V. This finding is in good agreement with C-V measurements. Based to C-V measurements (Fig. 1) the flat band voltage was found to be -5V. This in fact is a strong indication that the higher frequency relaxation is associated to the depletion region and it is due to the conductivity relaxation mechanism of this region.

IV. CONCLUSION

Silicon nitride MIS structures were characterized by means of Capacitance-Voltage and Conductance measurements. The devices exhibit rather low density of interface states. The G_p/ω versus frequency curves, appear to follow the 'extended tunneling' model in good agreement especially for the lower frequency data. The various relaxation mechanisms present under different bias conditions were examined by means of DRS. The results obtained were used in order to calculate the depletion width and the depletion resistance.

REFERENCES

- [1] N. Lusting and J. Kanicki, J. Appl. Phys., 1989, vol. 65, pp. 3951-3957.
- [2] F. Chen, B. Li, R. A. Dufresne, and R. Jammy, J. Appl. Phys., 2001, vol. 90, pp. 1898-1902.
- [3] B. S. Sahu, P. Srivastava, O. P. Agnihotri, and S. M. Shivaprasad, J. Non.Cryst. Solids, 2005, vol. 351, pp. 771-776.
- [4] M. Vila, C. Prieto, and R. Ramirez, Thin Solid Films, 2004, vol. 459, pp. 195-199.
- [5] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. Wiley, New York, 1981.
- [6] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts*, 2nd ed. Clarendon, Oxford, Appendix E, 1988.
- [7] Arash Takshi, Alexandros Dimopoulos, and John D. Madden, Appl. Phys. Lett., 2007, vol. 91, pp. 083513.
- [8] Eun-Chel Cho, Sangwook Park, Xiaojing Hao, Dengyuan Song, Gavin Conibeer, Sang-Cheol Park and Martin A. Green, Nanotechnology, 2008, vol. 19, pp. 245201.
- [9] C. Tsonos, I. Stavrakas, C. Anastasiadis, A. Kyriazopoulos, A. Kanapitsas, D. Triantis, J. Physics Chemistry Solids, 2009, vol. 70, pp.576-583.
- [10] V. Em. Vamvakas, N. Vourdas, S. Gardelis, Microelectron. Reliab., 2007, vol. 47, pp. 794-797.
- [11] D.Schroder, in "Semiconductor material and device characterization", 2nd. Ed. N.Y.: Wiley, 1998.
- [12] E.H.Nicollian, J.R. Brews, in "MOS Physics and Technology", Wiley, N.Y, 1982.
- [13] W.A.Hill, C.C.Coleman, Solid State Electronics, 1980, vol. 23, pp. 987-993.
- [14] N.Konofaos, Microelectronics Journal, 2004, vol. 35, pp. 421-425.
- [15] N.Konofaos, E.K.Evangelou, Semic. Sci. Technol., 2003, vol. 18, pp. 56-59.
- [16] D. Sands, K.M. Brunson, C.B. Thomas, Solid State Elect., 1987, vol. 30, pp. 543-548.
- [17] N. Konofaos, Semicond. Sci. Tech., 2001, vol. 16, pp. 733-738.